Single-Channel Power Distribution Switch

Description

The FP6861/B is a cost-effective, low voltage, single N-Channel MOSFET high-side power switch, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications.

The FP6861/B is equipped with a charge pump circuitry to drive the internal MOSFET switch. The switch's low $R_{DS(ON)}$, 90mΩ, meets USB voltage drop requirement, and a flag output is available to indicate fault conditions to the local USB controller.

Additional features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present, fault current is limited to specific current for FP6861/B in single port in accordance with the USB power requirements, lower quiescent current at 24μA making this device ideal for portable battery-operated equipment.

The FP6861/B is available in MSOP-8, SOP-8 and SOT-23-5 packages with smallest components.

Features

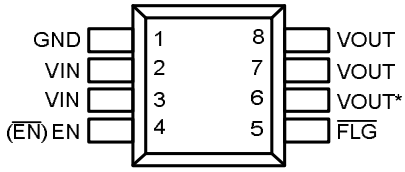
- Compliant to USB Specifications
- Built-In (Typically 90mΩ) N-Channel MOSFET
- Output Can Be Forced Higher Than Input (Off-State)
- Low Supply Current :
  24μA Typical at Switch On State
  1μA Typical at Switch Off State
- 400uS typical Rise Time
- Wide Input Voltage Ranges : 2.7V to 5.5V
- Open-Drain Fault Flag Output
- Hot Plug-In Application (Soft-Start)
- 2.5V Typical Under-Voltage Lockout (UVLO)
- Current Limiting Protection
- Thermal Shutdown Protection
- Reverse Current Flow Blocking (No Body Diode)
- Logic Level Enable Pin
- MSOP-8 ,SOP-8 and SOT-23-5 Packages
- RoHS Compliant
- UL Approved -E322418

Applications

- USB Bus/Self Powered Hubs
- USB Peripherals
- ACPI Power Distribution
- Notebook, Motherboard PCs
- Battery-Charger Circuits

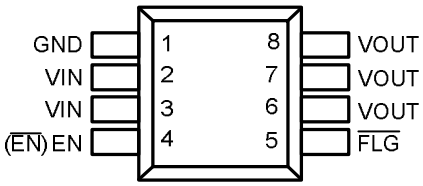
Pin Assignments

MS Package (MSOP-8)



*The pin 6 should be considered as VOUT when circuit design and PCB layout, but it is NC pin actually.

SO Package (SOP-8)

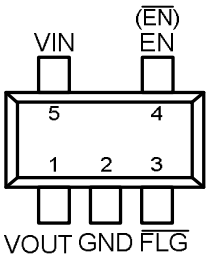


Ordering Information

FP6861B-□□□□□□

- TR: Tape / Reel
- G: Green
- Package Type
  MS: MSOP-8
  SO: SOP-8
  AS5: SOT-23-5
  BS5: SOT-23-5
- Enable
  1.Active High (Discharge)
  2.Active Low (Discharge)
  3.Active High (Non-Discharge)
  4.Active Low (Non-Discharge)
- Current Limit
  A:2A
  B:1.5A
  C:1A
  D:0.8A

AS5 Package (SOT-23-5)



BS5 Package (SOT-23-5)

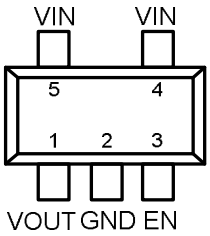


Figure1.Pin Assignment

SOT-23-5 Marking

Part Number	Product Code	Part Number	Product Code
FP6861B-C1AS5G	U0=	FP6861B-B1AS5G	Z7=
FP6861B-C2AS5G	U1=	FP6861B-B2AS5G	Y2=
FP6861B-C3AS5G	Y3=	FP6861B-B3AS5G	Z8=
FP6861B-C4AS5G	Y4=	FP6861B-B4AS5G	Z9=
FP6861B-C1BS5G	Y5=	FP6861B-B1BS5G	e8=
FP6861B-C2BS5G	Y6=	FP6861B-B2BS5G	e9=
FP6861B-C3BS5G	Y7=	FP6861B-B3BS5G	E4=
FP6861B-C4BS5G	Y8=	FP6861B-B4BS5G	E5=
FP6861B-A1BS5G	Y0=	FP6861B-D1AS5G	E6=
FP6861B-A2BS5G	Y9=	FP6861B-D2AS5G	h1=
FP6861B-A3BS5G	Z1=	FP6861B-D3AS5G	h2=
FP6861B-A4BS5G	Z2=	FP6861B-D4AS5G	h3=
FP6861B-A1AS5G	Z3=	FP6861B-D1BS5G	h4=
FP6861B-A2AS5G	Z4=	FP6861B-D2BS5G	h5=
FP6861B-A3AS5G	Z5=	FP6861B-D3BS5G	h6=
FP6861B-A4AS5G	Z6=	FP6861B-D4BS5G	h7=

Typical Application Circuit

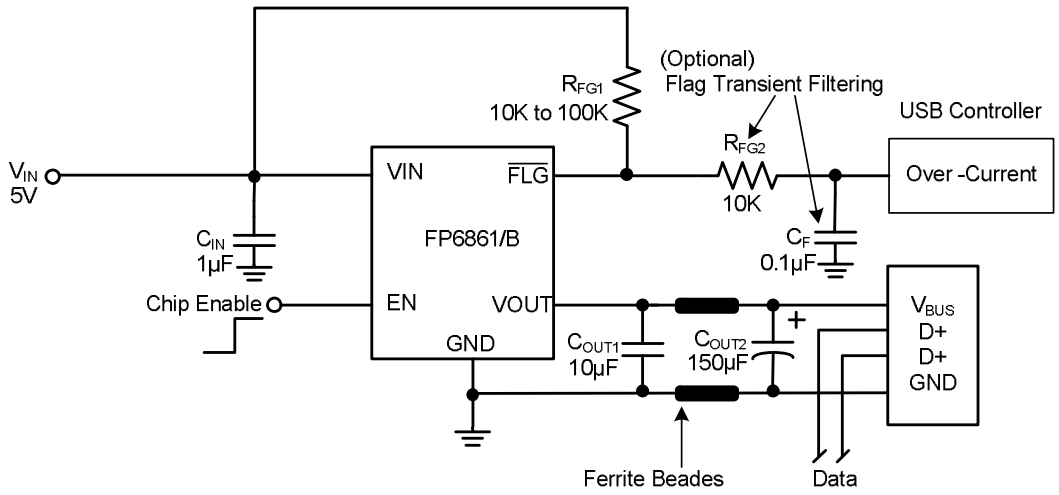


Figure 2. Typical Application Circuit

Functional Pin Description

Pin Name	Pin Function
VIN	Input Power Supply
VOUT	Switch Output
GND	Ground
EN	Chip Enable. Pull the pin high to enable IC; Pull the pin low to shutdown IC. Do not let the pin floating.
$\overline{\text{EN}}$	Chip Shutdown. Pull the pin high to shutdown IC; Pull the pin low to enable IC. Do not let the pin floating.
$\overline{\text{FLG}}$	Open-Drain Fault Flag Output

Block Diagram

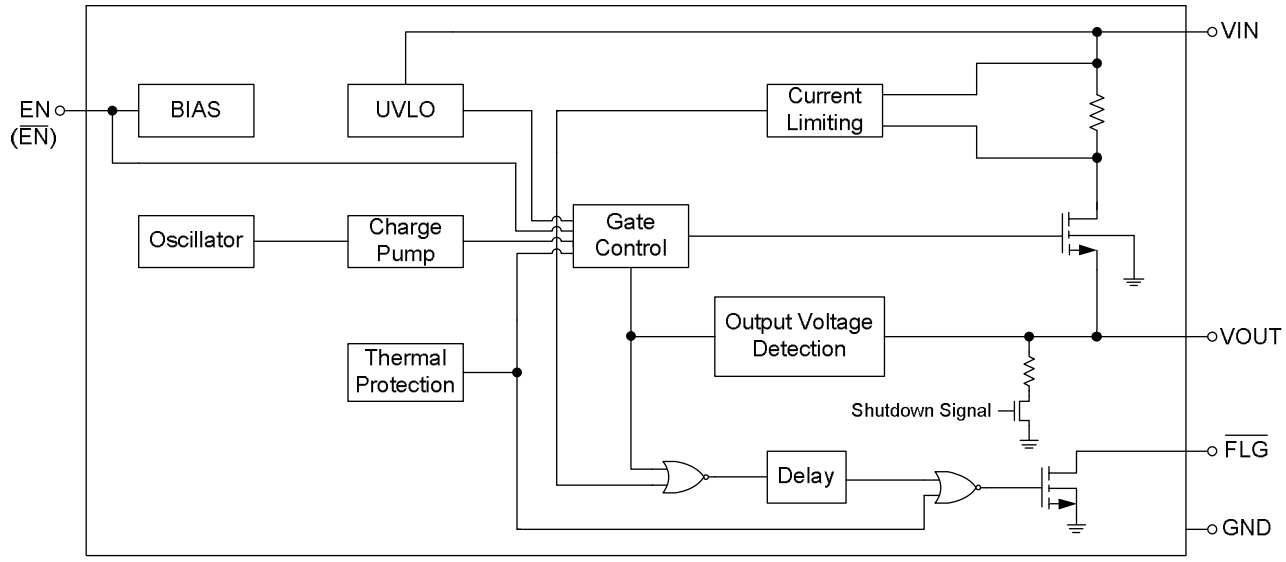


Figure 3. Block Diagram (Discharge Version)

Absolute Maximum Ratings

- VIN, VOUT---------- -0.3V to 6V
- EN (/EN)---------- -0.3V to 6V
- /FLG---------- -0.3V to 6V
- Power Dissipation @ T_A=25℃:
  - MSOP-8 (P_D)---------- +0.63W
  - SOP-8 (P_D) ---------- +0.63W
  - SOT-23-5 (P_D)---------- + 0.4W
- Package Thermal Resistance:
  - MSOP-8 (θ_{JA}) ---------- +160°C/W
  - SOP-8 (θ_{JA}) ---------- +160℃/W
  - SOT-23-5 (θ_{JA})---------- + 250℃/W
- Junction Temperature---------- +150℃
- Lead Temperature (Soldering,10 sec.)---------- +260℃
- Storage Temperature Range---------- -65℃ to +150℃

Note1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{IN})---------- +2.7V to +5.5V
- Operation Temperature Range (T_{OPR})---------- -40℃ to +85℃

Electrical Characteristics

(V_{IN}=5V, C_{IN}=C_{OUT}=1μF, T_A=25℃, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Switch On Resistance (Note2)	$R_{DS(ON)}$	I_{OUT}=1.0A		90	115	mΩ
Supply Current	I_{SW_ON}	Switch on, V_{OUT} = Open		24	40	μA
	I_{SW_OFF}	Switch off, V_{OUT} = Open		0.1	1	
EN Threshold	V_{IL}	Switch off			1.2	V
	V_{IH}	Switch on	1.8			
EN Input Current	I_{EN}	V_{EN} = 0V to 5.5V		0.01	0.1	μA
Output Leakage Current	$I_{LEAKAGE}$	V_{EN} = 0V, R_{LOAD} = 0Ω		0.5	1	μA
Output Turn-On Rise Time	T_{ON_RISE}	10% to 90% of V_{OUT} rising		400		μs
Current Limit	I_{LIM}	R_{LOAD} = 1Ω, FP6861BAX	1.5	2	2.8	A
		R_{LOAD} = 1Ω, FP6861BBX	1.1	1.5	2.1	A
		R_{LOAD} = 1Ω, FP6861BCX	0.7	1.0	1.4	A
		R_{LOAD} = 1Ω, FP6861BDX	0.53	0.8	1.28	A
Short Circuit Fold-Back Current	I_{SC_FB}	V_{OUT} = 0V, measured prior to thermal shutdown, FP6861BAX	0.2	1.3	1.9	A
		V_{OUT} = 0V, measured prior to thermal shutdown, FP6861BBX	0.2	1.0	1.4	A
		V_{OUT} = 0V, measured prior to thermal shutdown, FP6861BCX	0.2	0.67	1	A
		V_{OUT} = 0V, measured prior to thermal shutdown, FP6861BDX	0.2	0.53	0.75	A
FLAG Output Resistance	$R_{\overline{FLG}}$	I_{SINK} = 1mA		7	20	Ω
FLAG Off Current	$I_{\overline{FLG}\_OFF}$	$V_{\overline{FLG}}$ = 5V		0.01	0.1	μA
FLAG Delay Time	t_D	From fault condition to $\overline{FLG}$ assertion	5	10	20	ms
Under - Voltage Lockout	V_{UVLO}	V_{IN} increasing	2.2	2.5	2.7	V
Under - Voltage Hysteresis	ΔV_{UVLO}	V_{IN} decreasing		0.2		V
Shutdown Pull Low Resistance (Note3)	R_{PD}			50	150	Ω
Thermal Shutdown Threshold (Note2)	T_{SD}			135		℃
	ΔT_{SD}	Hysteresis		20		℃

Note2: Guarantee by design.
Note3: For discharge version.

Test Circuit

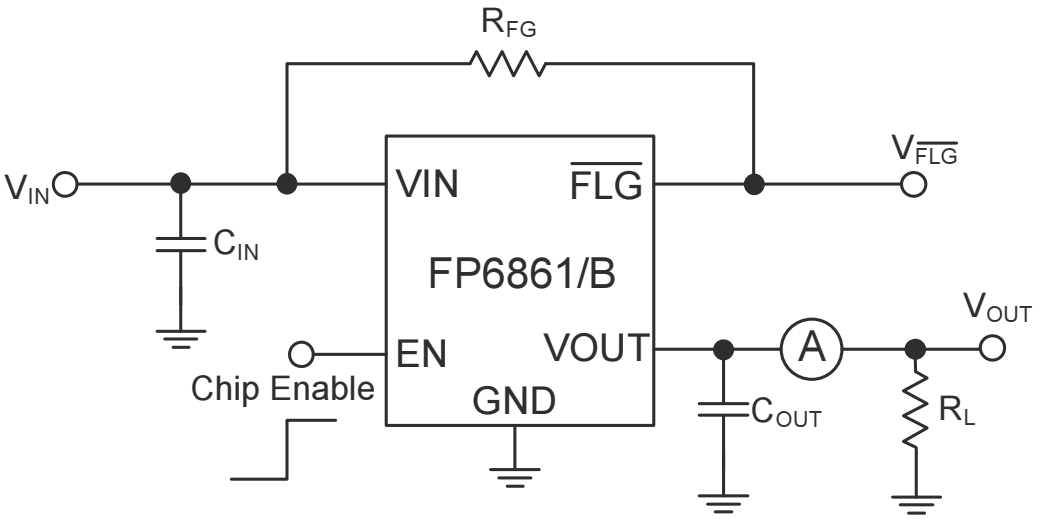


Figure 4.Electrical Characteristic Test Circuit of FP6861/B

Typical Performance Curves

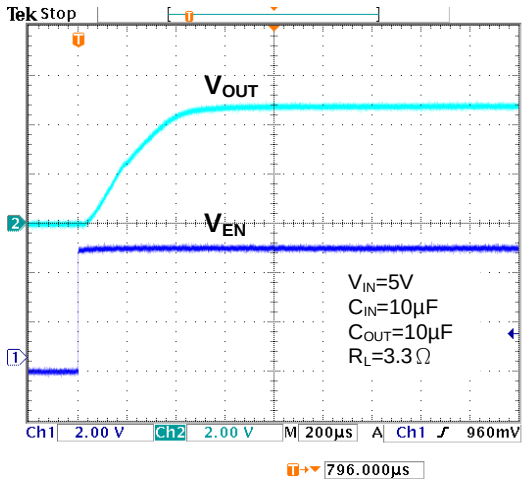


Figure 5. Turn-On Response

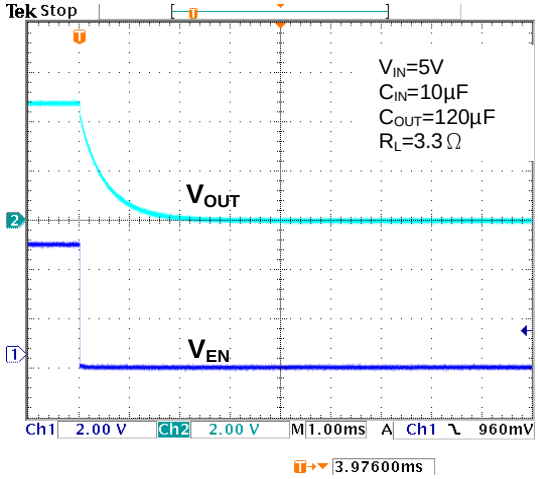


Figure 6. Turn-Off Response

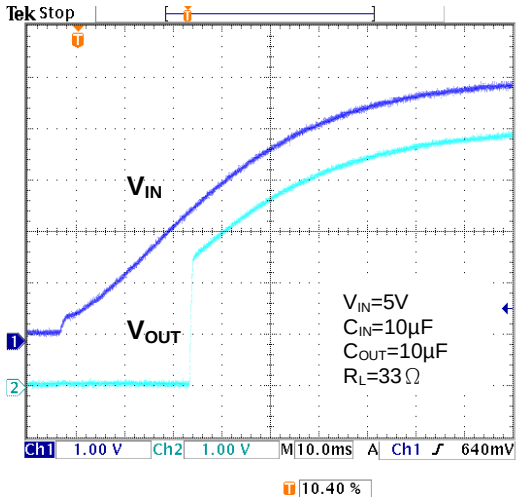


Figure 7. UVLO at Rising

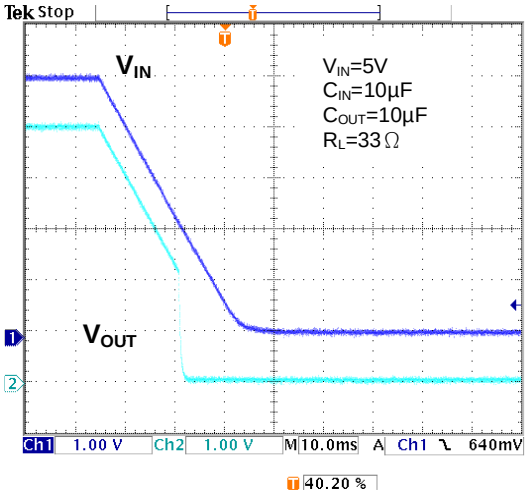


Figure 8. UVLO at Falling

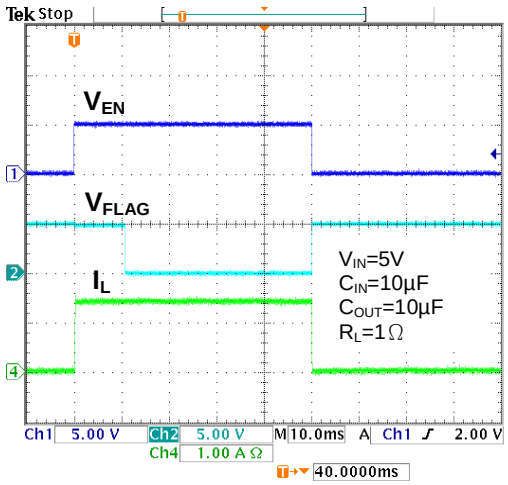


Figure 9. Flag Delay Response

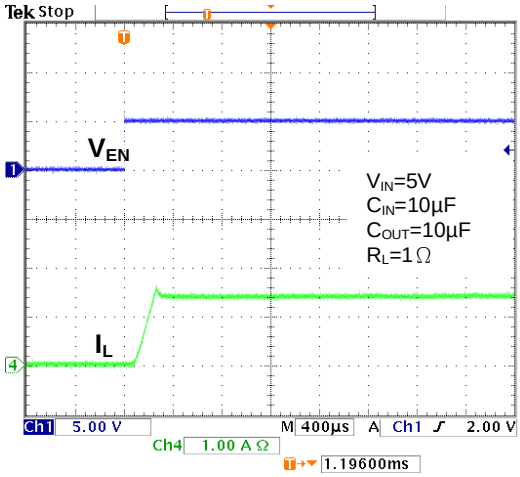


Figure 10. Current Limit Transient Response

Typical Performance Curves (Continued)

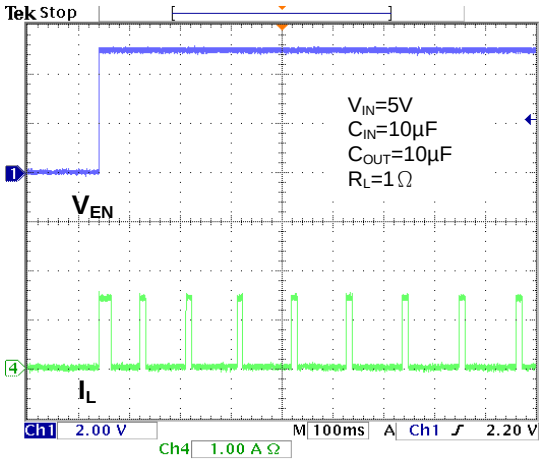


Figure 11. Thermal Shutdown

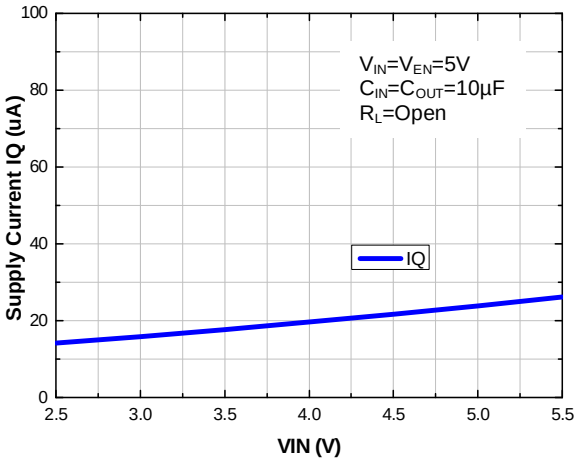


Figure 12. Supply Current vs. Input Voltage

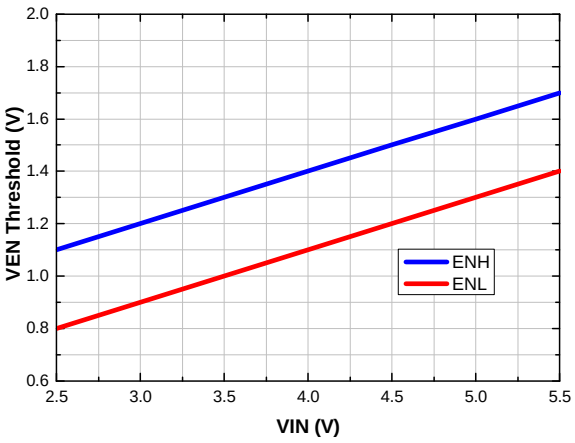


Figure 13. V_{EN} Threshold vs. Input Voltage

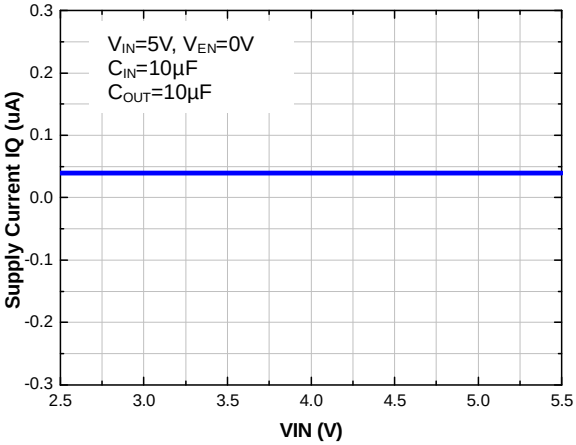


Figure 14. OFF Supply Current vs. Input Voltage

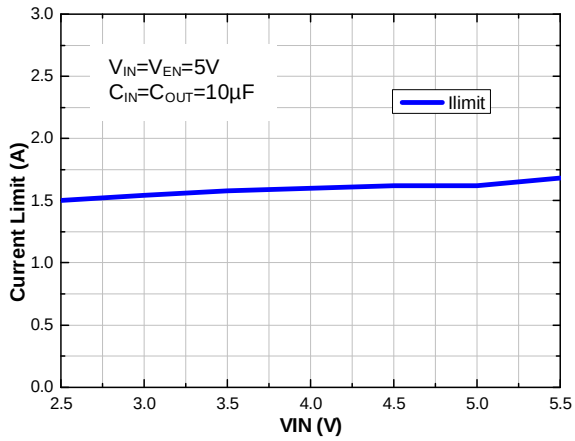


Figure 15.Current Limit vs. Input Voltage

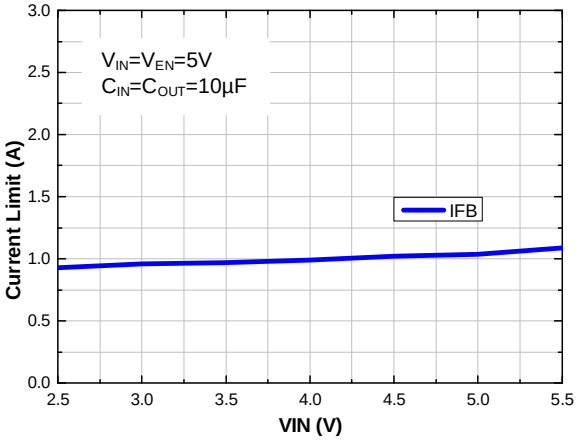


Figure 16.Current Fold-back vs. Input Voltage

Typical Performance Curves (Continued)

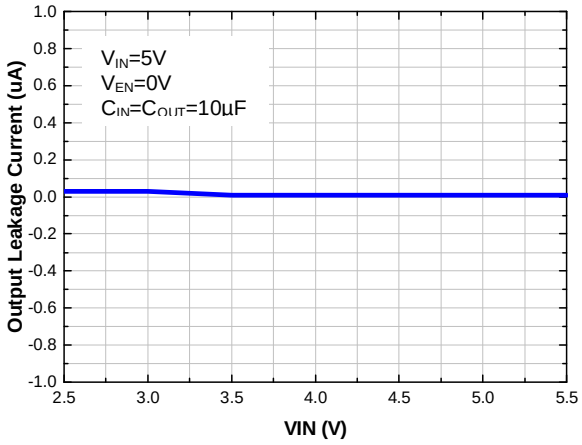


Figure 17. Output Leakage Current vs. Input Voltage

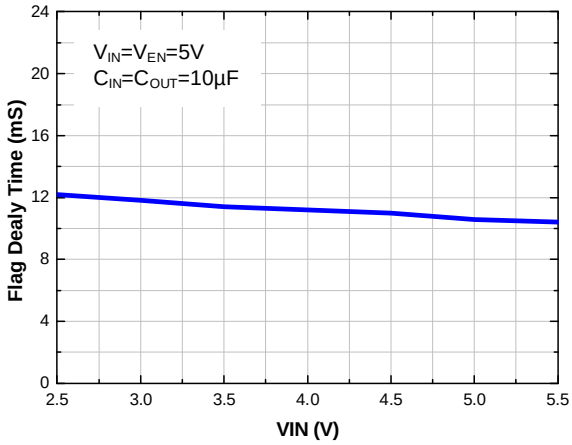


Figure 18. Flag Delay Time vs. Input Voltage

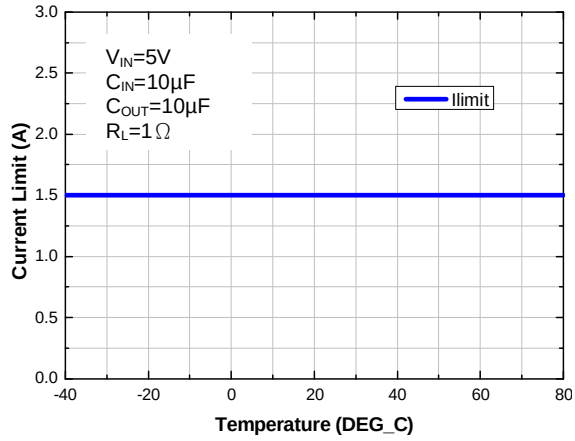


Figure 19. Current Limit vs. Temperature

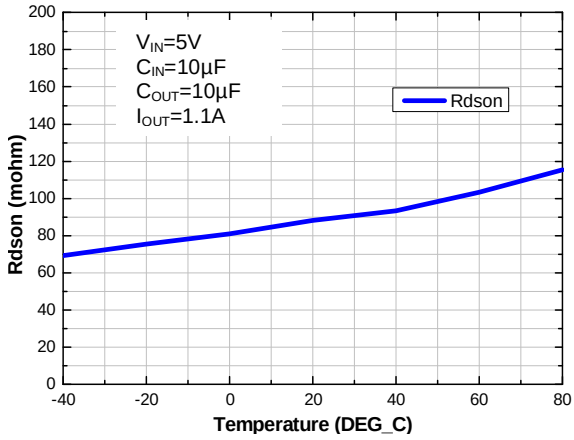


Figure 20. Rdson vs. Temperature

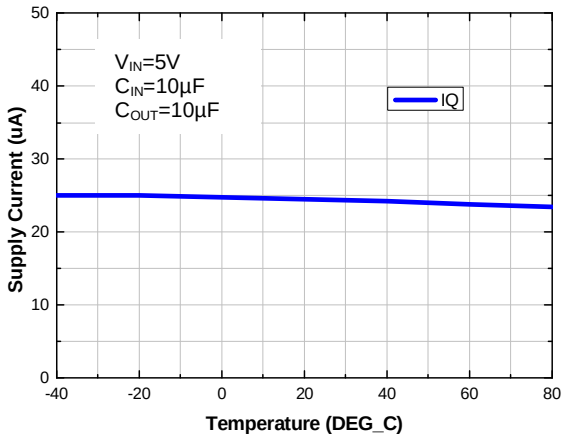


Figure 21. Supply Current vs. Temperature

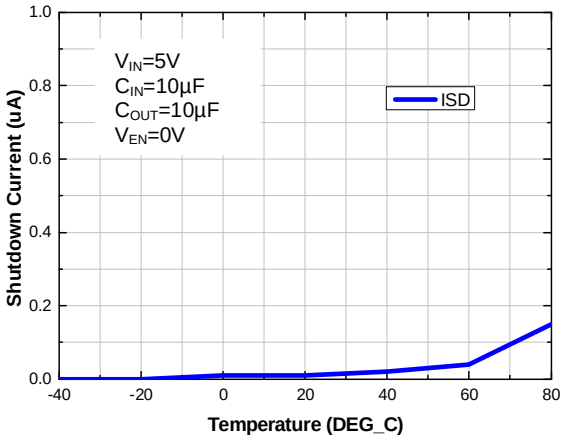


Figure 22. Shutdown Current vs. Temperature

Typical Performance Curves (Continued)

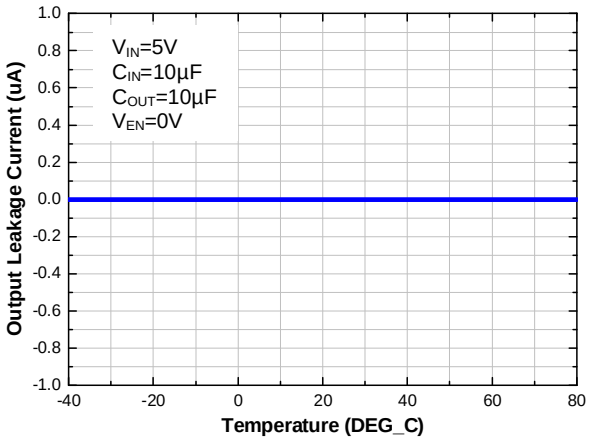


Figure 23. Output Leakage Current vs. Temperature

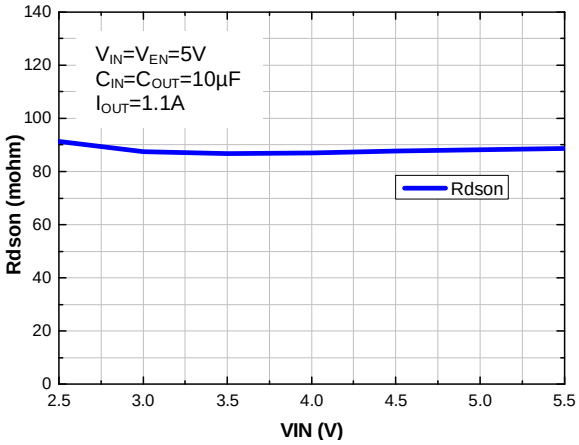


Figure 24. On-Resistance vs. Input Voltage

Application Information

The FP6861/B is a single N-Channel MOSFET high-side power switch with active-low enable input, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. The FP6861/B operates from 2.7V to 5.5V input voltage range and guarantees a minimum 1.1A output current. The switch's low $R_{DS(ON)}$, 90mΩ, meets USB voltage drop requirements. It has one switch with enable control input. The switch has an error flag output to notify the USB controller when the current-limit, short-circuit, under-voltage-lockout or thermal-shutdown occurs.

Under Voltage-Lockout

Under-voltage lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 2.5V. If input voltage drops below approximately 2.3V, UVLO turns off the MOSFET switch, /FLG will be asserted accordingly.

Thermal Shutdown

Thermal shutdown is employed to protect the device from damage if the die temperature exceeds safe margins due mainly to short-circuit or current-limit. Thermal shutdown shuts the switch off when current-limit or short-circuit occur and asserts the /FLG output if the die temperature reaches 135 ºC.

Reverse Current Blocking

The USB specification does not allow an output device to source current back into the USB port. However, the FP6861/B is designed to safely power noncompliant devices. When disable, the output is switched to a high-impedance state, blocking reverse current flow from the output back to the input. The switch is bidirectional when enable.

Error Flag

The FP6861/B provides an open drain error flag output for the switch. For most applications, connect /FLG to VIN through a pull-up resistor. /FLG goes low when any following condition occurs:

a. The thermal shutdown occurs.

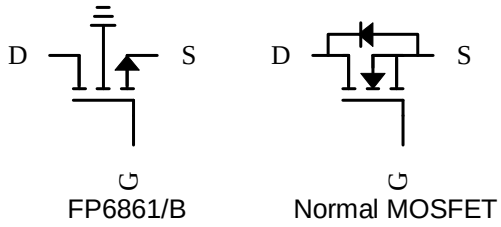
b. The switch is in current limit or short circuit conditions.

Fast Shutdown Load Discharge

The FP6861B provides a pull down resistance during EN is low, the resistance could discharge the load capacitor fast (refer to the block diagram).

Input and Output

VIN is the power source connection to the internal circuitry and the drain of the MOSFET. VOUT is the source of the MOSFET. In typical application, current flows through the switch from VIN to VOUT toward the load. If VOUT is greater than VIN, current will flow from VOUT to VIN since the MOSFET is bidirectional. There is no a parasitic body diode between drain and source of the MOSFET, the FP6861/B prevents reverse current flow if VOUT externally forced a higher voltage than VIN when the output disabled (V_{EN} < 1.2V).



FP6861/B Normal MOSFET

Chip Enable input

The switch will be disabled when the EN pin is in a logic low condition. During this condition, the internal circuitry and MOSFET are turned off, reducing the supply current to 0.1uA typical. The maximum guaranteed voltage for a logic low at the EN pin is 1.2V. A minimum guaranteed voltage of 1.8V at the EN pin will turn the FP6861/B on. Floating the input may cause unpredictable operation.

Soft Start for Hot Plug-In Application

In order to eliminate the upstream voltage droop caused by the large inrush current during hot-plug events, the “soft-start” feature effectively isolates the power source from extremely large capacitive loads, satisfying the USB voltage droop requirements.

Application Information (Continued)

Fault Flag

The FP6861/B provides a /FLG signal pin which is an N-Channel open drain MOSFET output. This open drain output goes low when VOUT < VIN-1V, current limit or the die temperature exceeds 135°C approximately. The /FLG output is capable of sinking a 10mA load to typically 200mV above ground. The /FLG pin requires a pull-up resistor; this resistor should be large in value to reduce energy drain. A 100kΩ pull-up resistor works well for most applications. In the case of an over-current condition, /FLG will be asserted only after the 10ms flag response delay time. This ensures that /FLG is asserted only upon valid over-current conditions and that erroneous error reporting is eliminated.

For example, false over-current conditions may occur during hot-plug events when extremely large capacitive loads are connected and causes a high transient inrush current that exceeds the current limit threshold.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold of typically 1.5A through the switch of FP6861/B. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

Voltage Drop

The USB specification states a minimum port-output voltage in two locations on the bus, 4.75V out of a Self-Powered Hub port and 4.4V out of a Bus-Powered Hub port. As with the Self-Powered Hub, all resistive voltage drops for the Bus-Powered Hub must be accounted for to guarantee voltage regulation.

The following calculation determines $V_{OUT\ (MIN)}$ for multiple ports (N_{PORT}) ganged together through one switch:

$$V_{OUT\ (MIN)} = 4.75V - [I_{OUT} \times (4 \times R_{CON} + 2 \times R_{CAB})] - (0.1A \times N_{PORT} \times R_{SWITCH}) - V_{DROP}$$

where:

R_{CON}: Resistance of connector contacts

(two contacts per connector)

R_{CAB}: Resistance of upstream cable wires

(one 5V and one GND)

R_{SWITCH}: Resistance of power switch

(100mΩ typical for FP6861/B)

V_{DROP} : PCB voltage drop

Supply Filter/Bypass Capacitor

A 10uF low-ESR ceramic capacitor from VIN to GND, located at the device is strongly bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. The input transient must not exceed 6V of the absolute maximum supply voltage even for a short duration.

Output Filter Capacitor

A low-ESR 150uF aluminum electrolytic or tantalum between VOUT and GND is strongly recommended to meet the 330mV maximum droop requirement in the hub V_{BUS} (Per USB 2.0, output ports must have a minimum 120uF of low-ESR bulk capacitance per hub). Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused when downstream cables are hot-insertion transients. Ferrite beads in series with V_{BUS}, the ground line and the 0.1uF bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies.

Application Information (Continued)

Power Dissipation

The device's junction temperature depends on several factors such as the load, PCB layout, ambient temperature and package type. The output pin of FP6861/B can deliver a current up to 1.1A, respectively over the full operating junction temperature range. However, the maximum output current must be decreased at higher ambient temperature to ensure the junction temperature does not exceed 160°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the $R_{DS(ON)}$ of switch as below.

$$P_D = R_{DS(ON)} \times (I_{OUT})^2$$

Although the devices are rated for 1.1A of output current, but the application may limit the amount of output current based on the total power dissipation and the ambient temperature. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$P_{D\,(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-5 packages, the thermal resistance θ_{JA} is 250°C/W on the standard JEDEC 51-3 single-layer thermal test board.

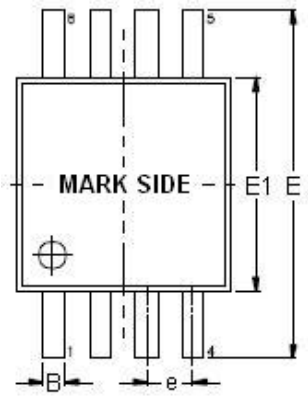
PCB Layout

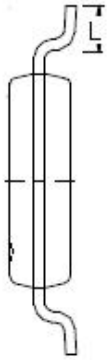
In order to meet the voltage drop, droop, and EMI requirements, careful PCB layout is necessary. The following guidelines must be considered:

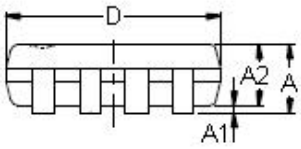
- Keep all V_{BUS} traces as short as possible and use at least 50-mil, 2 ounce copper for all V_{BUS} traces.
- Locate the FP6861/B as close as possible to the output port to limit switching noise.
- Locate the ceramic bypass capacitors as close as possible to the VIN pins of the FP6861/B.
- Avoid vias as much as possible. If vias are necessary, make them as large as feasible.
- Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance (Use a separate ground and power plans if possible).
- Place cuts in the ground plane between ports to help reduce the coupling of transients between ports.
- Locate the output capacitor and ferrite beads as close to the USB connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient load performance.

Outline Information

MSOP- 8 Package (Unit: mm)



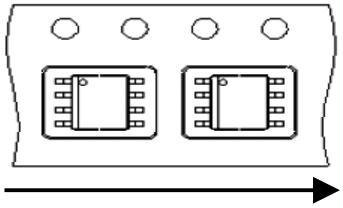




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.80	1.10
A1	0.05	0.15
A2	0.75	0.95
B	0.25	0.35
D	2.90	3.10
E	4.80	5.00
E1	2.90	3.10
e	0.60	0.70
L	0.40	0.80

Note : Followed From JEDEC MO-187-E.

Taping Orientation

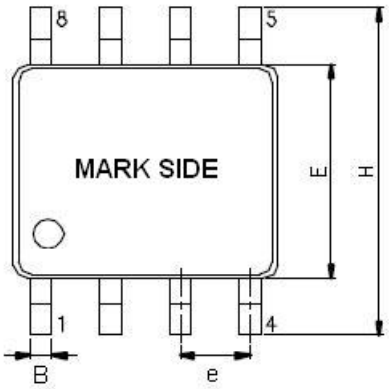


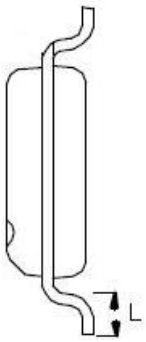
Feed Direction

Typical MSOP Package

Outline Information (Continued)

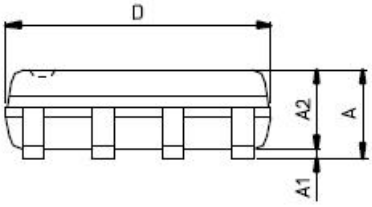
SOP- 8 Package (Unit: mm)



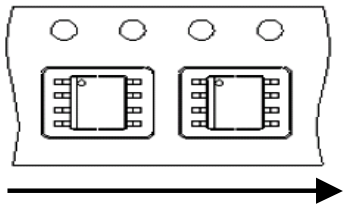


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.35	1.75
A1	0.05	0.25
A2	1.30	1.50
B	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note：Followed From JEDEC MO-012-E



Taping Orientation

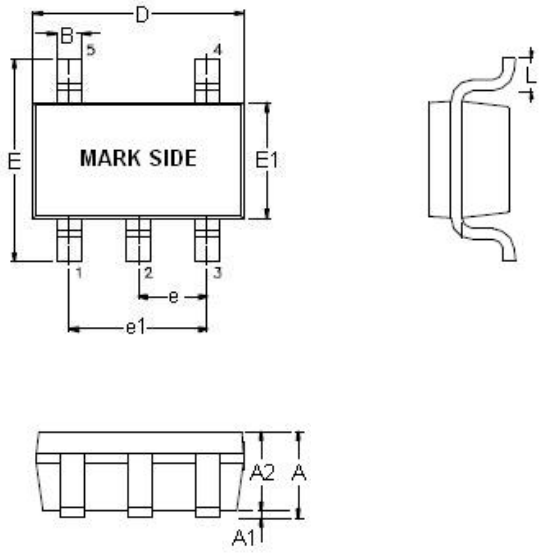


Feed Direction

Typical SOP Package

Outline Information (Continued)

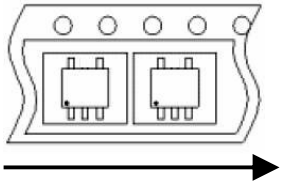
SOT-23-5 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.00	1.20
A1	0.00	0.10
A2	1.00	1.10
B	0.35	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.35	0.55

Note：Followed From JEDEC MO-178-C.

Taping Orientation



Feed Direction

Typical SOT Package